**[0016]** FIG. **1** is a simplified schematic diagram of circuit **20** wherein ESD clamp **21** is placed, for example, between input-output (I/O) terminal **22** and ground or common terminal **23** of an IC to protect other devices therein, that is, to protect "circuit core" **24** also coupled to I/O and common terminals **22**, **23**. Person of skill in the art will understand that ESD clamp **21** may be placed across any terminals of the IC, and reference herein to I/O terminals is intended to include any and all other terminals not merely those used for input or output signals. Further, the Zener diode symbol illustrated in block **21** of FIG. **1** is merely for convenience of identifying the voltage limiting function of ESD block **21** and not intended to imply that a Zener diode is necessarily present therein. With respect to structures or elements used for ESD protection, the terms device, clamp and transistor are used interchangeably.

**[0017]** FIG. **2** is a simplified schematic diagram illustrating internal components of ESD clamp **21** employing bipolar transistor **25**, having emitter **26**, collector **27**, base **28**, and internal resistance **29**, coupled across I/O terminals **22**, **23**. When the voltage across terminals **22**, **23** rises beyond a predetermined limit, bipolar transistor **25** turns on, limiting the voltage across terminals **22**, **23**, desirably to a level below that capable of damaging circuit core **24**.

**[0018]** FIG. **3** shows simplified plot **30** of transmission line pulse current (I) versus voltage (V) for a typical electrostatic discharge (ESD) protection device such as, for example, device **21** of FIG. **2**. As the applied voltage is increased, very little current flows until triggering voltage **31** is reached at voltage Vt**1**. Once triggered into operation, the ESD device conducts and the current increases to holding point **32** with current Ih and voltage Vh. Depending upon the internal impedance of the voltage source, current and voltage may further increase to point **33** at current It**2** and voltage Vt**2**, beyond which destructive failure may occur leading to further current increase accompanied by voltage decrease.

**[0019]** Electrostatic discharge (ESD) protection devices are intended to remain quiescent during normal operation of the associated semiconductor (SC) device(s) or non-SC device(s) or integrated circuit (IC) (i.e., the protected element (s) or circuit core **24**) having a normal operating voltage Vo, but turn on when excessive voltage arises, thereby preventing damage to the protected element(s). The triggering voltage Vt**1** of the ESD device should exceed the maximum normal DC operating voltage Vo(MAX) of the protected elements, otherwise the ESD device will interfere with normal operation of the protected elements. Further, Vt**1** should be less than, for example, a voltage $V_{TR}$ (usually a transient voltage) large enough to damage the protected element(s), hereafter referred to as the protected element break-down voltage, abbreviated as $V_{TR}$(PEBD). Thus, the ESD device should be designed so that Vo(MAX)<Vt**1**<$V_{TR}$(PEBD). It is commonplace to provide a number of ESD clamps **21** on a SC die or wafer so that all of the various terminals of the IC or electronic assembly may be protected. It is usually important that the Vt**1** values for these several ESD clamps be similar or lie within a narrow predetermined range.

**[0020]** When bipolar transistor **25** of FIG. **2** is used for ESD clamp **21**, the triggering voltage Vt**1** is heavily influenced by the base-collector spacing of transistor **25**. Unfortunately, it is often the case that even though several clamp transistors **25** are manufactured at the same time on the same SC wafer or die using nominally the same mask shapes and dimensions, there can be significant variation in the base-collector spacing in different parts of the SC wafer and/or die as a function, for example, of the azimuthal orientation of transistor **25** on the wafer or die. This has the result that Vt**1** of nominally identical clamp devices can be different in different regions of the same IC, depending, for example, on their relative azimuthal orientation on the IC wafer or die. This Vt**1** variation (hereafter ΔVt**1**) can adversely affect overall manufacturing yield and is not desirable. In the past, various process modifications have been used to minimize ΔVt**1**, but such modifications are often accompanied by an undesirable increase in manufacturing cost or other difficulties.

**[0021]** Accordingly, there is an ongoing need to provide improved ESD clamps that operate at more consistent triggering voltages Vt**1** independent of their location or orientation on a particular IC die or wafer, that is, to minimize ΔVt**1**. Further, it is desirable that the improved ESD clamps be obtainable without significant modification of the manufacturing process used for forming the ESD clamps and the associated circuit core of the IC. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this background of the invention.

**[0022]** FIG. **4** shows a simplified cross-sectional view of ESD clamp transistor **70** implemented in a semiconductor substrate according to an embodiment of the present invention. Transistor **70** is formed in substrate **72** (e.g. P) having buried layer region **73** therein (e.g., N type, abbreviated as NBL **73**). Overlying NBL **73** is region **74** extending from NBL **73** to upper surface **71**. Region **74** may be either N or P. depending upon the particular process available and the desired devices being fabricated at the same time. Hence, region **74** is identified in the various drawings as being "N/P" indicating that either conductivity type may be used. In a preferred embodiment, P type is used. Within region **74** are shallow trench dielectric isolation (STI) regions **79** having interface **791** with the underlying semiconductor, WELL regions **761** and **762** (e.g., N type, collectively **76**) with contact region **80** (e.g., N+) in region **762**, and WELL region **75** (e.g., P type) with lateral interface or boundary **751**. Further N region **86** is provided in electrical contact with N WELL region **762** with lateral interface or boundary **861** facing toward interface **751** of P WELL region **75** and separated therefrom by distance D. Doped contact region **77** (e.g., P+) is provided in P WELL region **75** to make Ohmic contact to P WELL region **75**. Doped region **78** (e.g., N+) in P WELL region **75** serves as the emitter of transistor **70**. P WELL region **75** serves as the base of transistor **70**. N WELL regions **86**, **762** with N+ contact region **80** serve as the collector of transistor **70**. Intermediate portion **85** of region **74** lies between interfaces or boundaries **751**, **861** separated by distance D. As will be subsequently explained, intermediate portion **85** of region **74** is more lightly doped than adjacent regions **75** and **86**. As the voltage applied between terminals **22**, **23** of transistor **70** approaches avalanche conditions, more lightly doped intermediate portion **85**, whether of N or P type, becomes substantially depleted of free carriers, and effectively defines the base-collector spacing. Hence, for convenience of explanation, distance D across intermediate portion **85** between boundaries **751**, **861** is referred to herein as the base-collector spacing irrespective of whether portion **85** is N type or P type. Dielectric layer **81** is conveniently provided on surface (e.g., interface) **71** with openings therein extending to